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(54) **PIXEL CIRCUIT AND ELECTROLUMINESCENT DISPLAY INCLUDING THE SAME**

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(57) **ABSTRACT**

A pixel circuit and an electroluminescent display including the same are disclosed. In one aspect, the pixel circuit includes a scan transistor connected between a data line and a first node and having a gate electrode configured to receive a scan signal, a driving transistor connected between a first power supply voltage and a third node and having a gate electrode connected to a second node, an emission control transistor connected between the third node and a fourth node and having a gate electrode configured to receive an emission control signal, a light-emitting diode connected between the fourth node and a second power supply voltage less than the first power supply voltage, and a compensation circuit initializes the second node to an initial voltage during a first compensation period and electrically connects the second node to the third node during a second compensation period following the first compensation period.

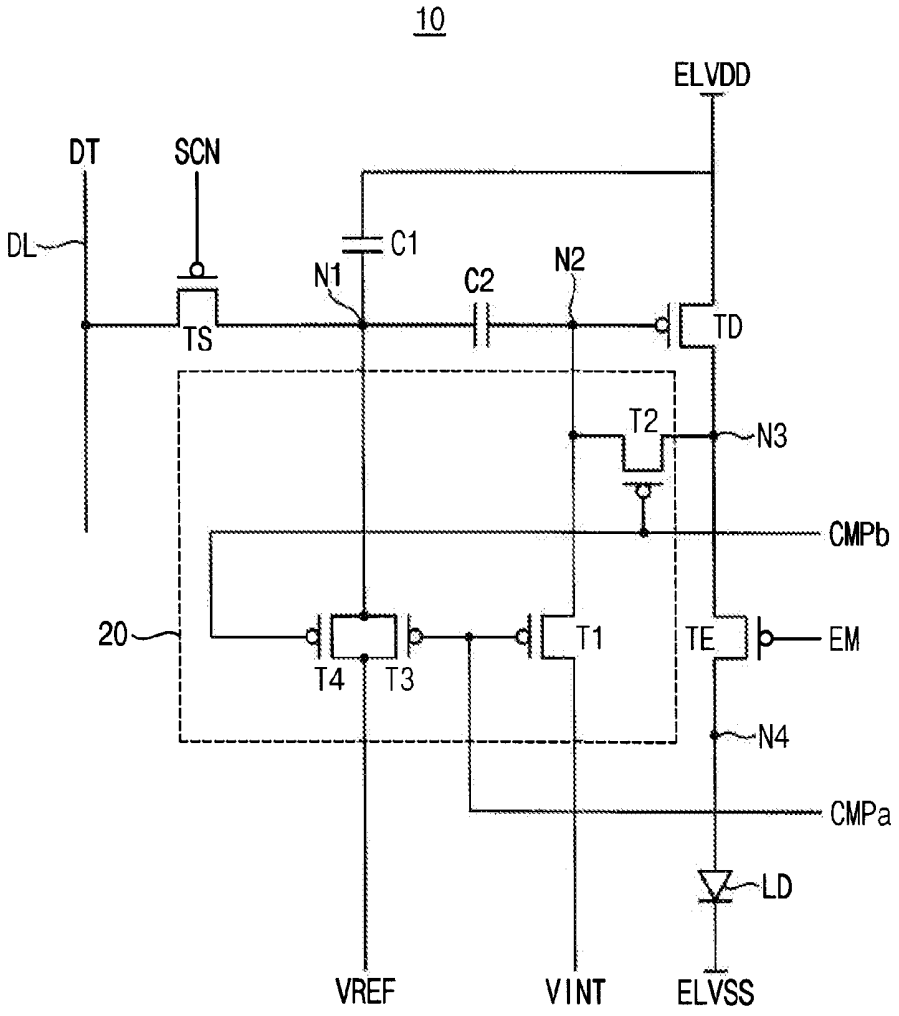
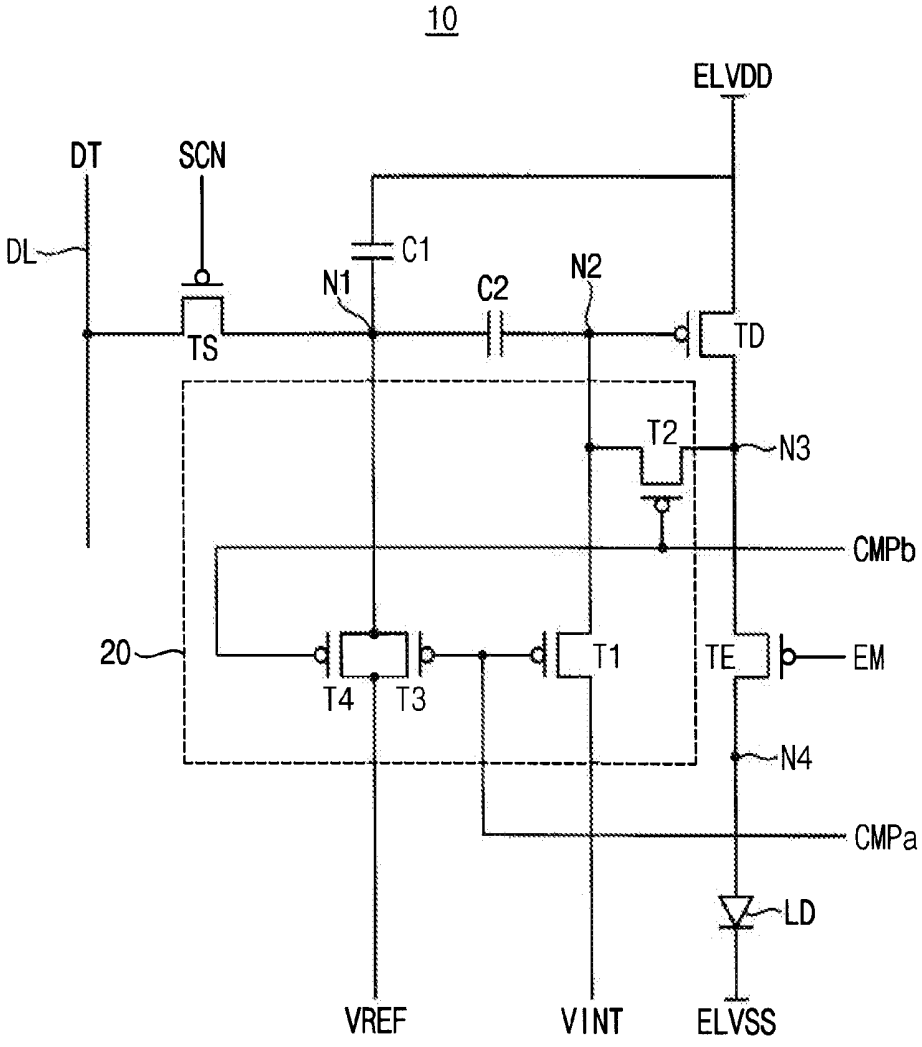


FIG. 1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ELVDD
DT
SCN
DL
C1
N1
C2
N2
TS
TD
T2
N3
CMPb
20
T4
T3
T1
TE
EM
N4
CMPa
LD
VREF
VINT
ELVSS

FIG. 2

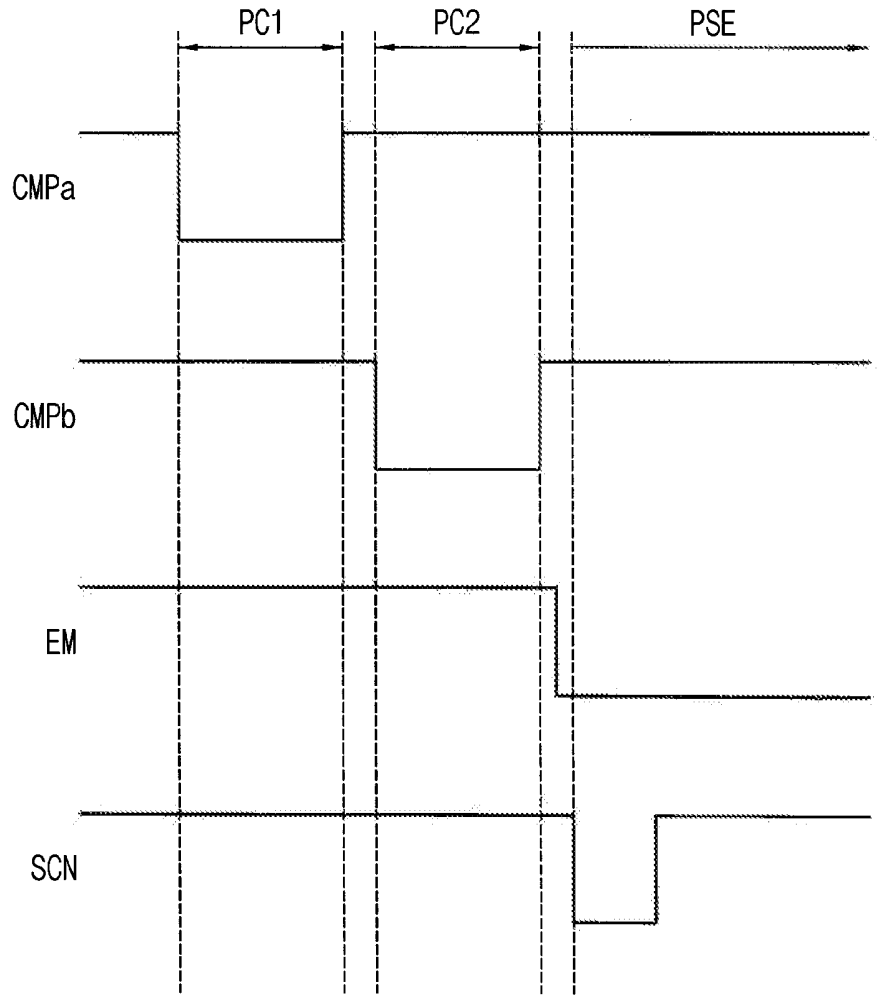
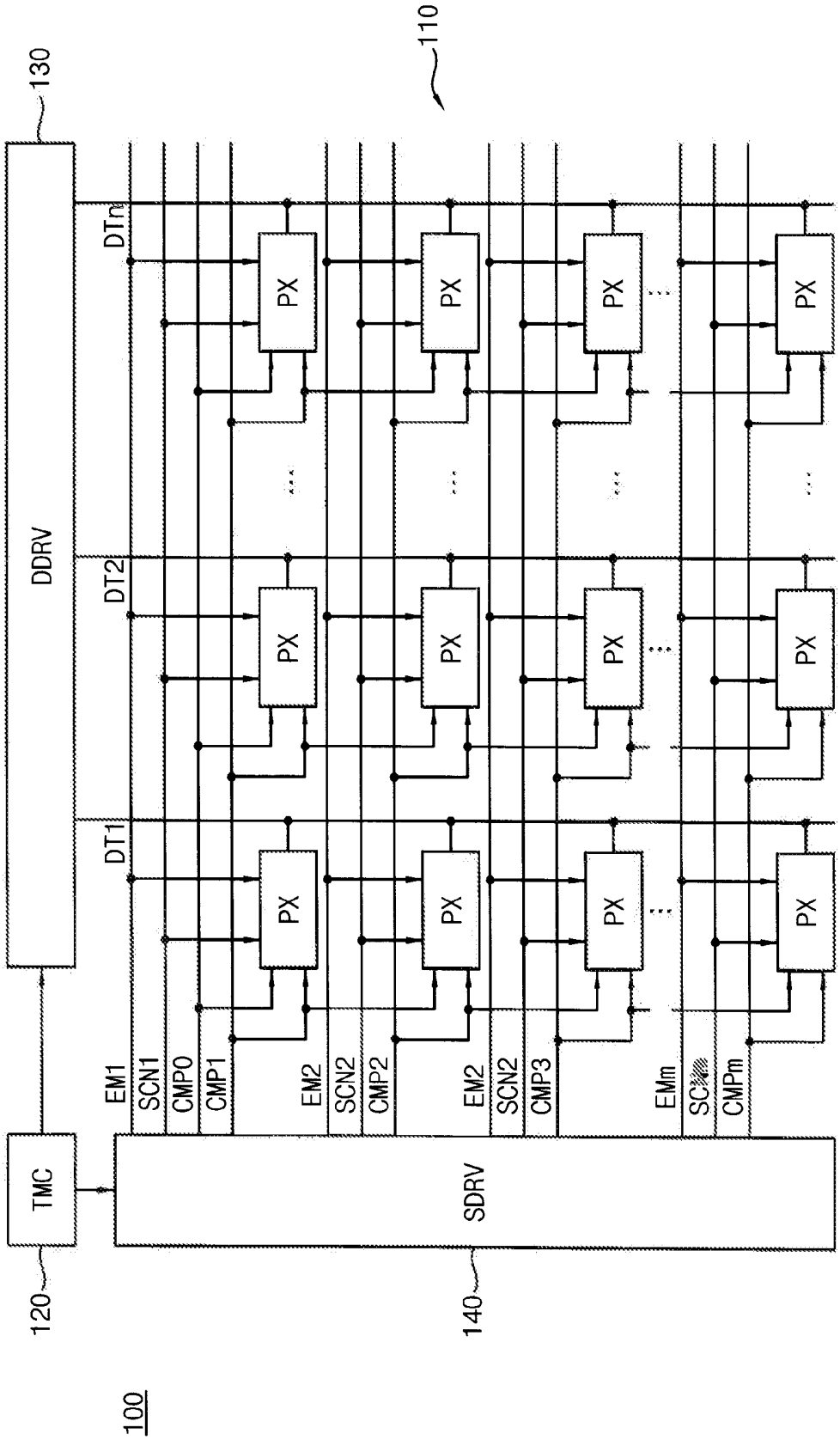


FIG. 3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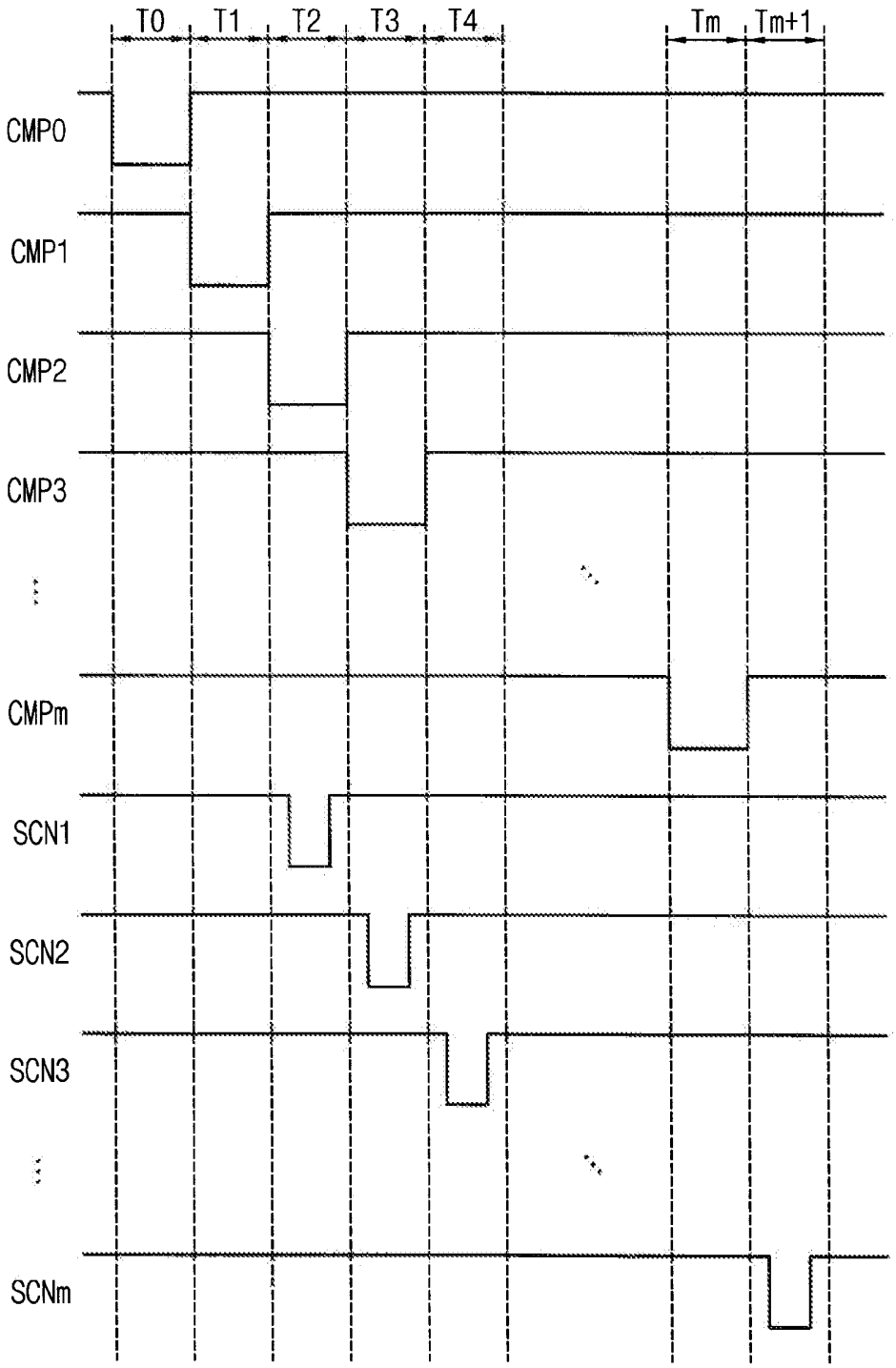
110
120
130
140
TMC
DDRV
SDRV
DT1
DT2
DTn
EM1
SCN1
CMP0
CMP1
EM2
SCN2
CMP2
EM2
SCN2
CMP3
EMm
SCN2
CMPm
PX

FIG. 4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T3
T4
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Tm+1
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CMPm
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SCN2
SCN3
SCNm

FIG. 5

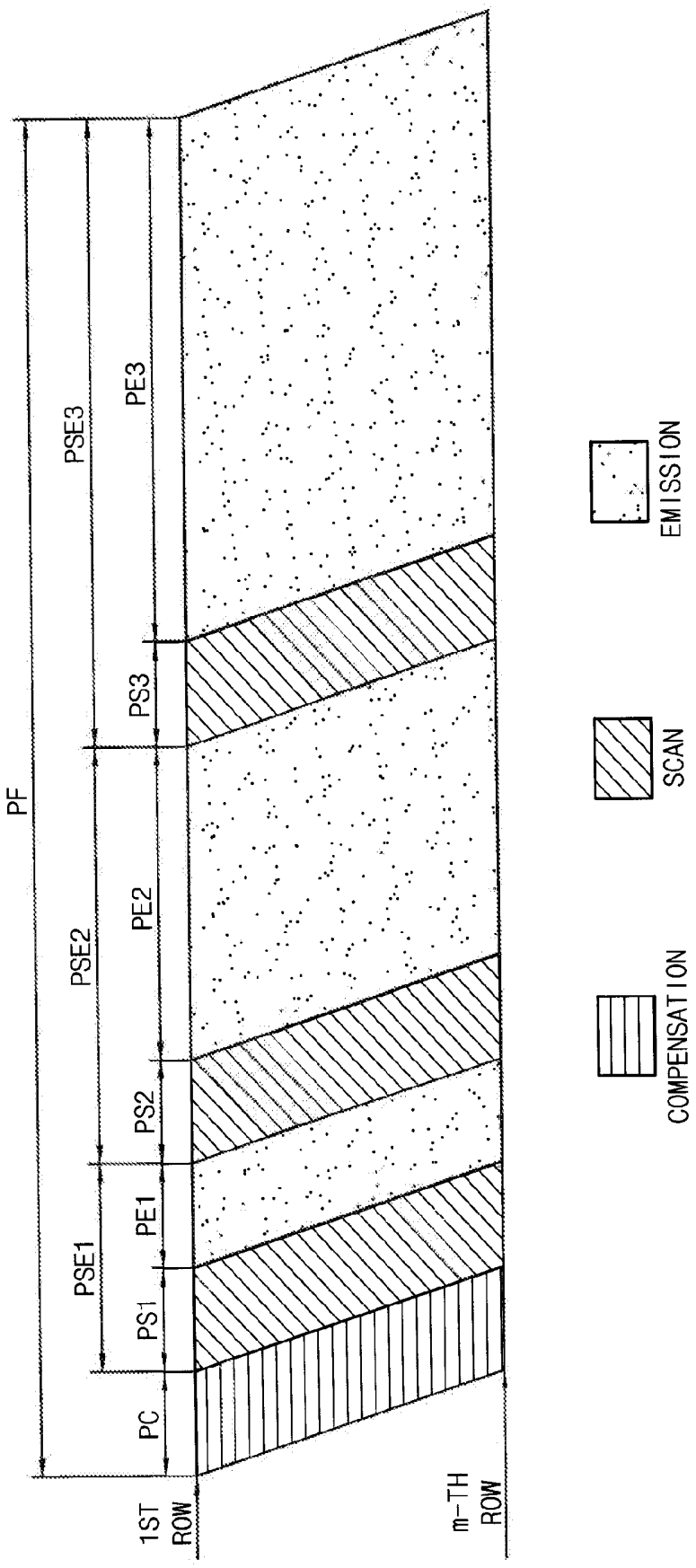
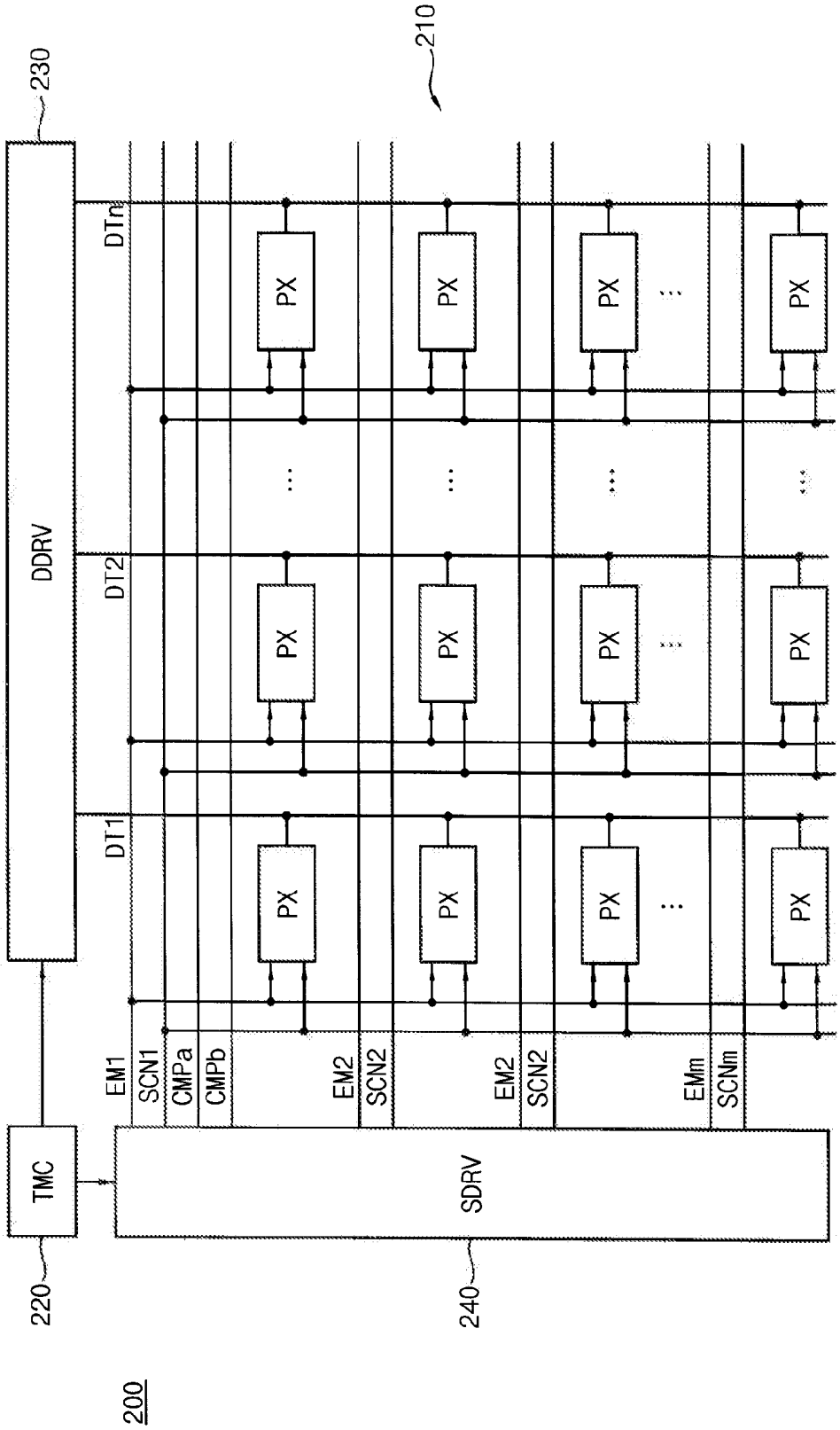

PF
PSE3
PE3
PS3
PSE2
PE2
PS2
PSE1
PE1
PS1
PC
1ST ROW
m-TH ROW
EMISSION
SCAN
COMPENSATION

FIG. 6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230
240
TMC
DDRV
SDRV
DT1
DT2
DTm
EM1
SCN1
CMPa
CMPb
EM2
SCN2
EM2
SCN2
EMm
SCNm
PX

FIG. 7

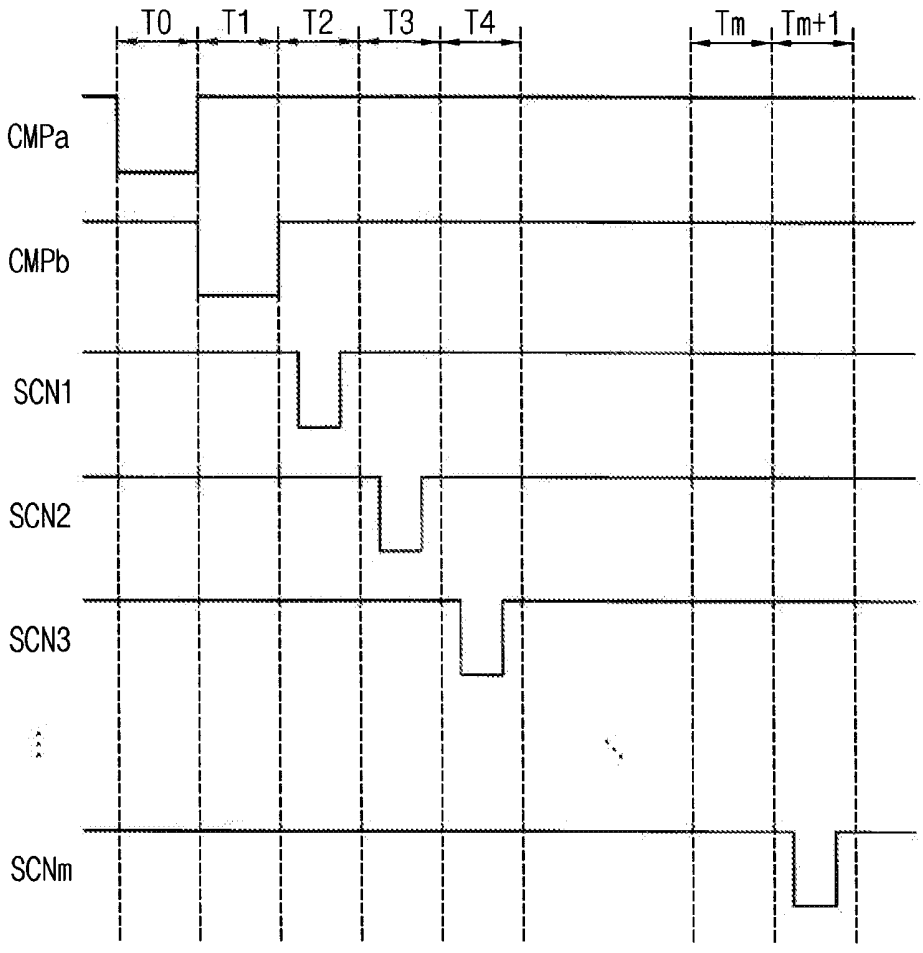


FIG. 8

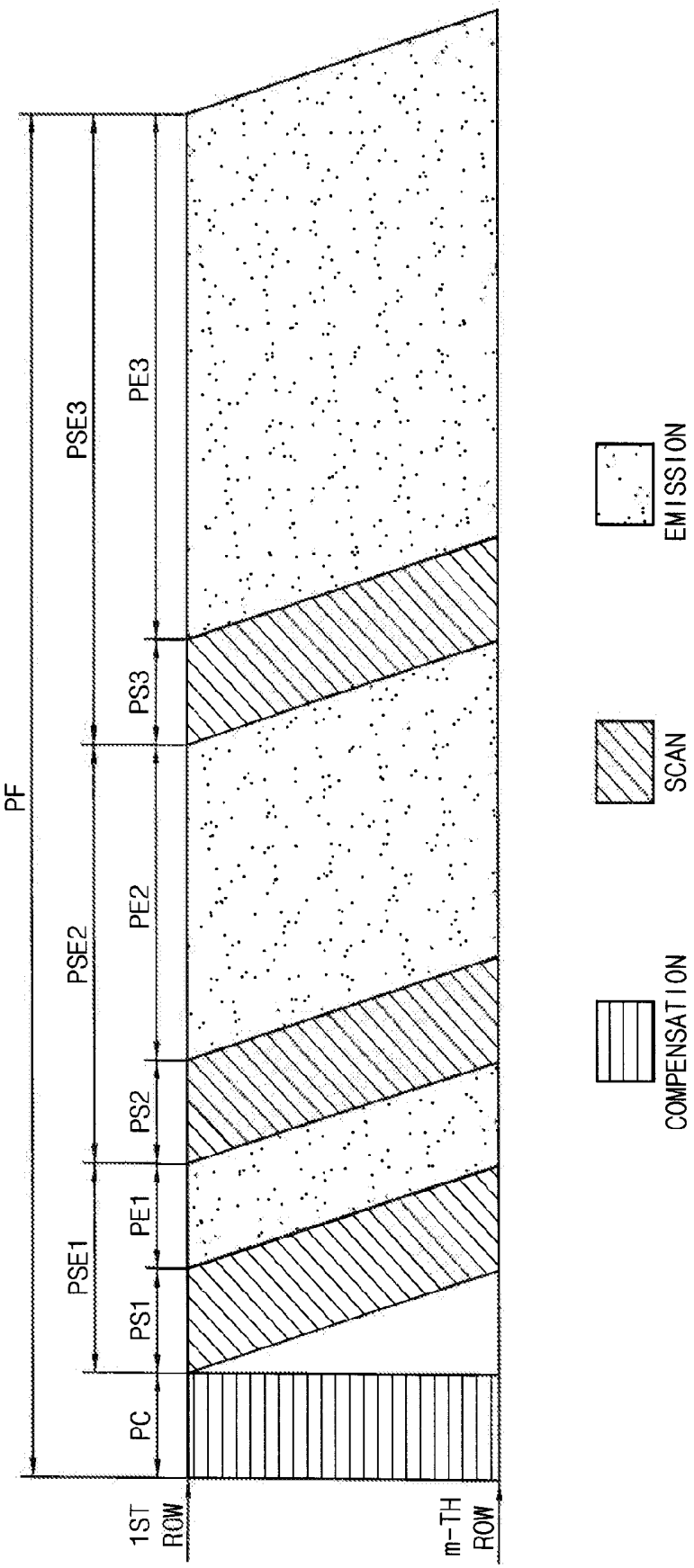

PF
PSE3
PE3
PS3
PSE2
PE2
PS2
PSE1
PE1
PS1
PC
1ST ROW
m-TH ROW
EMISSION
SCAN
COMPENSATION

FIG. 9

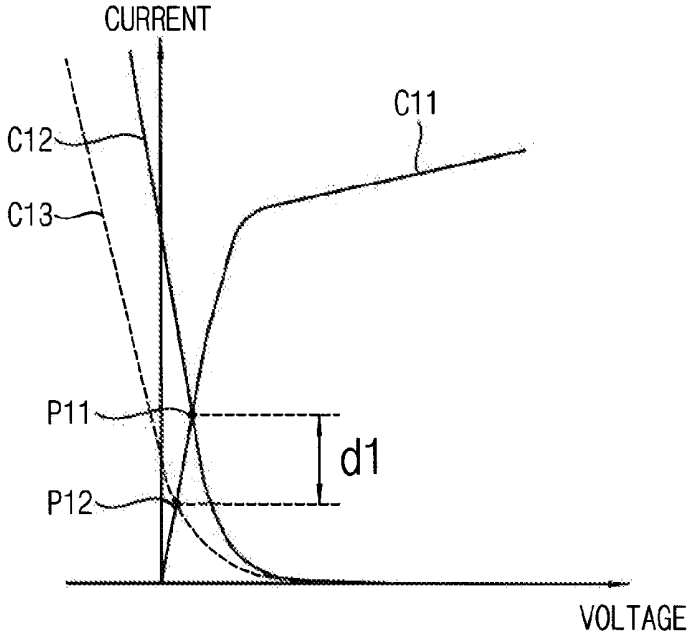

CURRENT
C11
C12
C13
P11
d1
P12
VOLTAGE

FIG. 10

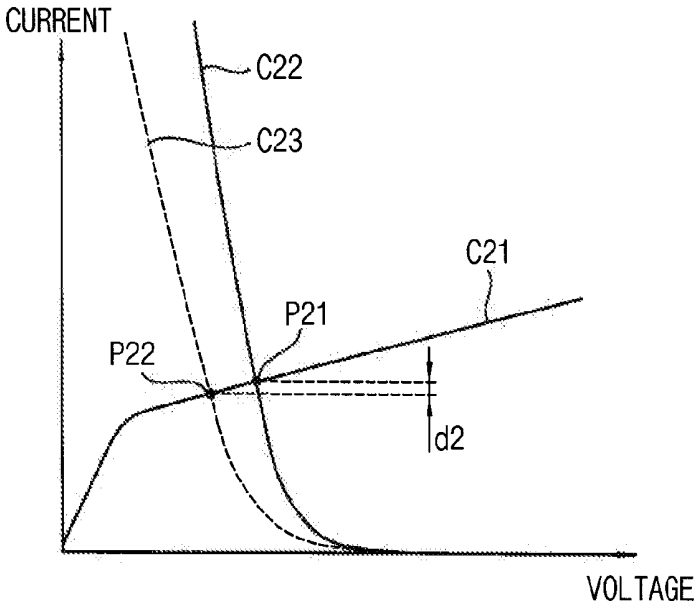

CURRENT
C22
C23
C21
P21
P22
d2
VOLTAGE

FIG. 11

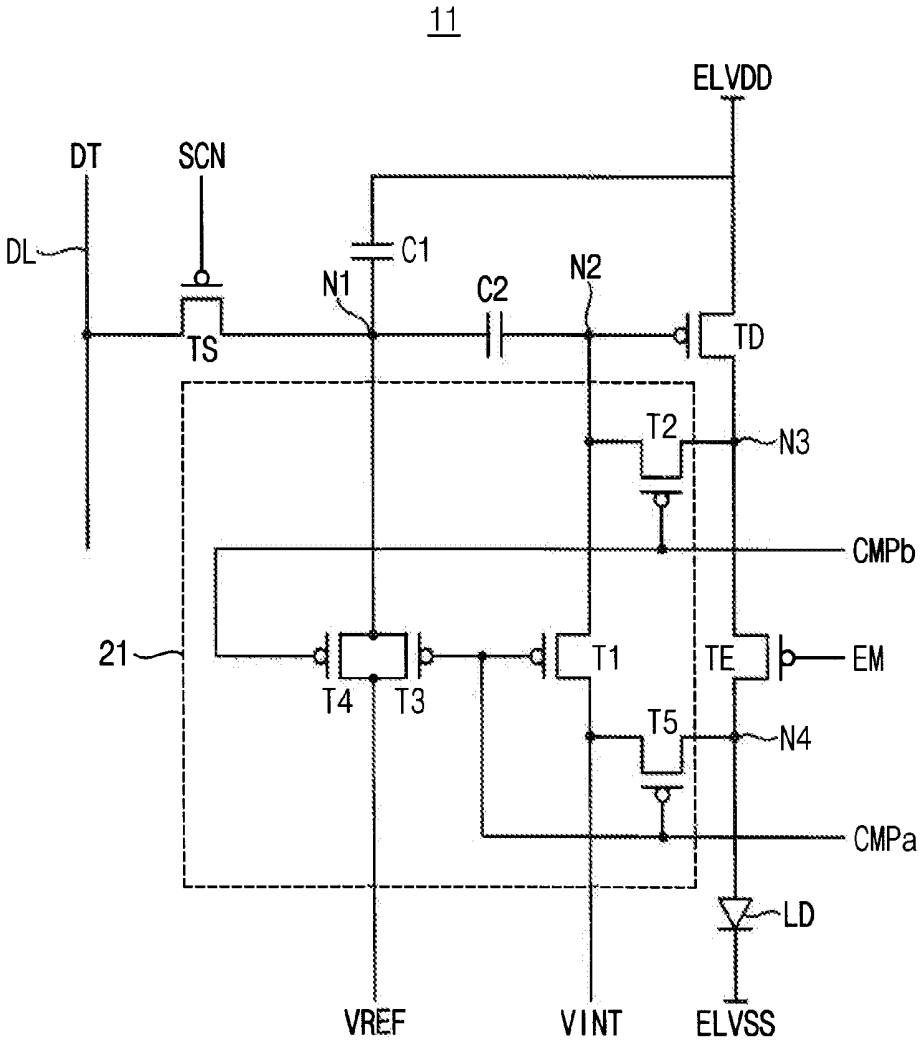
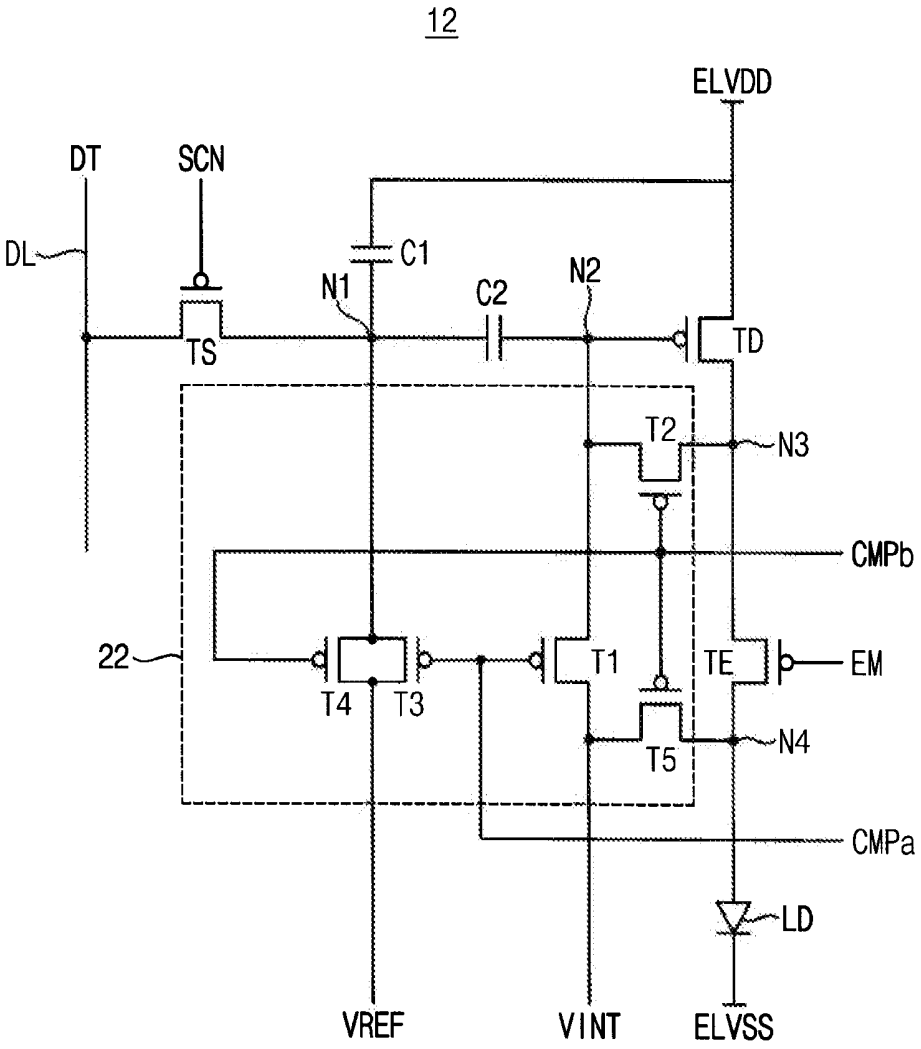

11
ELVDD
DT
SCN
DL
C1
N1
C2
N2
TS
TD
T2
N3
CMPb
21
T1
TE
EM
T4
T3
T5
N4
CMPa
LD
VREF
VINT
ELVSS

FIG. 12


12
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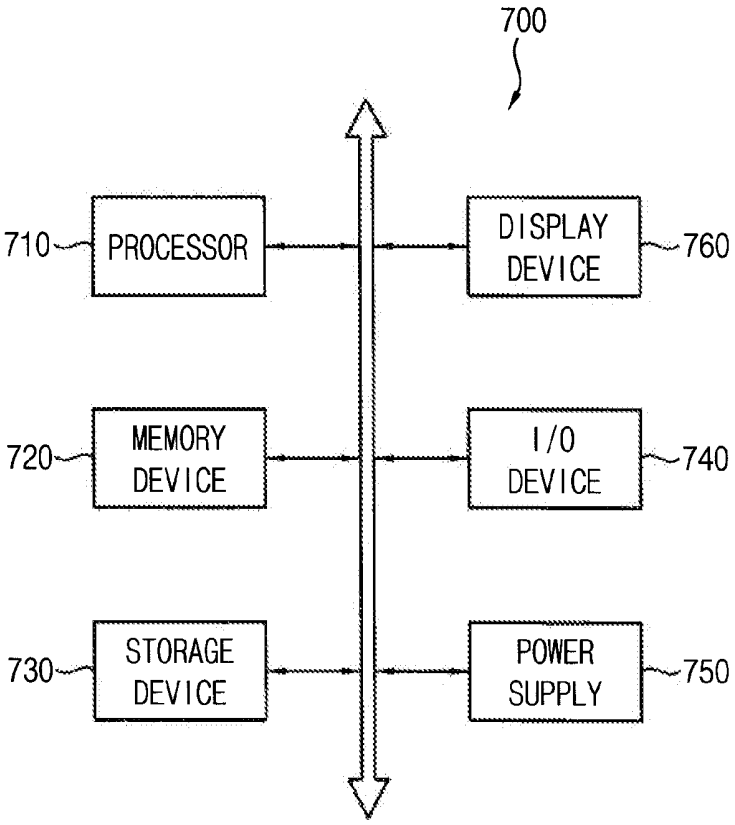
DT
SCN
DL
C1
N1
C2
N2
TS
TD
T2
N3
CMPb
22
T4
T3
T1
TE
EM
T5
N4
CMPa
LD
VREF
VINT
ELVSS

FIG. 13


700
710
PROCESSOR
DISPLAY DEVICE
760
720
MEMORY DEVICE
I/O DEVICE
740
730
STORAGE DEVICE
POWER SUPPLY
750

PIXEL CIRCUIT AND ELECTROLUMINESCENT DISPLAY INCLUDING THE SAME

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application claims priority under 35 U.S.C. §119 to Korean Patent Application No. 10-2014-0065307 filed on May 29, 2014, the disclosure of which is hereby incorporated by reference herein in its entirety.

BACKGROUND

[0002] 1. Field

[0003] The described technology generally relates to a pixel circuit and an electroluminescent display including the pixel circuit.

[0004] 2. Description of the Related Art

[0005] Recently, various display devices such as liquid crystal displays (LCD), plasma displays, and electroluminescent displays have gained popularity. Particularly, the electroluminescent display can be driven with quick response speed and reduced power consumption, using a light-emitting diode (LED) or an organic light-emitting diode (OLED) that emits light through recombination of electrons and holes.

[0006] The electroluminescent display can be driven with an analog or a digital driving method. While the analog driving method produces grayscale using variable voltage levels corresponding to input data, the digital driving method produces grayscale using variable time duration in which the LED emits light. The analog driving method is difficult to implement because it requires a driving integrated circuit (IC) that is complicated to manufacture if the display is large and has high resolution. The digital driving method, on the other hand, can readily accomplish the required high resolution through a simpler IC structure.

SUMMARY OF CERTAIN INVENTIVE ASPECTS

[0007] One inventive aspect is a pixel circuit that is robust to variation factors such as change of temperature and/or voltage, deviation in threshold voltage of a driving transistor, degradation of a light emitting diode, etc.

[0008] Another aspect is an electroluminescent display device including the pixel circuit robust to the variation factors.

[0009] Another aspect is a pixel circuit of an electroluminescent display device that includes, a scan transistor, a first capacitor, a second capacitor, a driving transistor, an emission control transistor, a light emitting diode and a compensation circuit. The scan transistor is coupled between a data line and a first node, and a gate electrode of the scan transistor receives a scan signal. The first capacitor is coupled between a first power supply voltage and the first node. The second capacitor is coupled between the first node and a second node. The driving transistor is coupled between the first power supply voltage and a third node, and a gate electrode of the driving transistor is coupled to the second node. The emission control transistor is coupled between the third node and a fourth node, and a gate electrode of the emission control transistor receives an emission control signal. The light emitting diode is coupled between the fourth node and a second power supply voltage that is lower than the first power supply voltage. The compensation circuit initializes the second node to an initial voltage during a first compensation period and electrically connects the second node and the third node during a second compensation period after the first compensation period.

[0010] The compensation circuit can apply a reference voltage to the first node during the first compensation period and the second compensation period.

[0011] The driving transistor can be turned on when a data voltage is lower than the reference voltage and the driving transistor is turned off when the data voltage is higher than the reference voltage.

[0012] The compensation circuit can apply the initial voltage to the fourth node during the first compensation period or the second compensation period.

[0013] Each frame period can include the first compensation period, the second compensation period after the first compensation period, and a scan period after the second compensation period, and the scan transistor can be turned on during the scan period.

[0014] The initial voltage can be lower than the first power supply voltage subtracted by a threshold voltage of the driving transistor.

[0015] The initial voltage can be equal to the second power supply voltage.

[0016] The compensation circuit can include a first transistor and a second transistor. The first transistor can be coupled between the second node and the initial voltage, and a gate electrode of the first transistor can receive a first compensation control signal that is activated during the first compensation period. The second transistor can be coupled between the second node and the third node, and a gate electrode of the second transistor can receive a second compensation control signal that is activated during the second compensation period.

[0017] The compensation circuit can further include a third transistor and a fourth transistor. The third transistor can be coupled between the first node and a reference voltage, and a gate electrode of the third transistor can receive the first compensation control signal. The fourth transistor can be coupled between the first node and the reference voltage, and a gate electrode of the fourth transistor can receive the second compensation control signal.

[0018] The compensation circuit can further include a fifth transistor coupled between the fourth node and the initial voltage, and a gate electrode of the fifth transistor can receive the first compensation control signal or the second compensation control signal.

[0019] The driving transistor can operate in a saturation region.

[0020] Another aspect is an electroluminescent display device that includes a display unit, a data driver, a scan driver and a timing controller. The display unit includes a plurality of pixel circuits that are arranged in rows and columns. Each pixel circuit is configured to initialize a gate electrode of a driving transistor to an initial voltage during a first compensation period and electrically connect the gate electrode and a drain electrode of the driving transistor during a second compensation period after the first compensation period. The data driver provides data signals to the display unit and the scan driver provides row control signals to the display unit. The timing controller controls the display unit, the data driver and the scan driver.

[0021] The scan driver can generate a plurality of compensation control signals that are activated sequentially.

[0022] A (k−1)-th compensation control signal and a k-th compensation control signal among the plurality of compensation control signals can be provide to the pixel circuits of a k-th row.

[0023] Each pixel circuit of the k-th row can initialize the gate electrode of the driving transistor to the initial voltage while the (k−1)-th compensation control signal is activated and electrically connect the gate electrode and the drain electrode of the driving transistor while the k-th compensation control signal is activated.

[0024] The scan driver can generate a first compensation control signal and a second compensation control signal that are activated sequentially.

[0025] The first compensation control signal and the second compensation control signal can be provided commonly to the pixel circuits of all rows.

[0026] Each pixel circuit of all rows can initialize the gate electrode of the driving transistor to the initial voltage while the first compensation control signal is activated and electrically connect the gate electrode and the drain electrode of the driving transistor while the second compensation control signal is activated.

[0027] Each pixel circuit include a scan transistor, a first capacitor, a second capacitor, a driving transistor, an emission control transistor, a light emitting diode and a compensation circuit. The scan transistor is coupled between a data line and a first node, and a gate electrode of the scan transistor receives a scan signal. The first capacitor is coupled between a first power supply voltage and the first node. The second capacitor is coupled between the first node and a second node. The driving transistor is coupled between the first power supply voltage and a third node, and the gate electrode of the driving voltage is coupled to the second node. The emission control transistor is coupled between the third node and a fourth node, and a gate electrode of the emission control transistor receiving an emission control signal. The light emitting diode is coupled between the fourth node and a second power supply voltage that is lower than the first power supply voltage. The compensation circuit is configured to initialize the second node to an initial voltage during the first compensation period and electrically connect the second node and the third node during the second compensation period after the first compensation period.

[0028] The compensation can circuit include first through fourth transistors. The first transistor can be coupled between the second node and the initial voltage, and a gate electrode of the first transistor can receive a first compensation control signal that is activated during the first compensation period. The second transistor can be coupled between the second node and the third node, and a gate electrode of the second transistor can receive a second compensation control signal that is activated during the second compensation period. The third transistor can be coupled between the first node and a reference voltage, and a gate electrode of the third transistor can receive the first compensation control signal. The fourth transistor can be coupled between the first node and the reference voltage, and a gate electrode of the fourth transistor can receive the second compensation control signal.

[0029] Another aspect is a pixel circuit for an electroluminescent display comprising a scan transistor connected between a data line and a first node and having a gate electrode configured to receive a scan signal, a first capacitor connected between a first power supply voltage and the first node, a second capacitor connected between the first node and a second node, a driving transistor connected between the first power supply voltage and a third node and having a gate electrode connected to the second node, an emission control transistor connected between the third node and a fourth node and having a gate electrode configured to receive an emission control signal, a light-emitting diode (LED) connected between the fourth node and a second power supply voltage less than the first power supply voltage, and a compensation circuit configured to i) initialize the second node to an initial voltage during a first compensation period and ii) electrically connect the second node to the third node during a second compensation period following the first compensation period.

[0030] In the above pixel circuit, the compensation circuit is further configured to apply a reference voltage to the first node during the first and second compensation periods. In the above pixel circuit, the driving transistor is configured to be turned on when a data voltage on the data line is less than the reference voltage, wherein the driving transistor is configured to be turned off when the data voltage is greater than the reference voltage.

[0031] In the above pixel circuit, the compensation circuit is further configured to apply the initial voltage to the fourth node during the first or second compensation period.

[0032] In the above pixel circuit, the first and second compensation periods and a scan period after the second compensation period are defined as a frame period of the electroluminescent display, wherein the scan transistor is configured to be turned on during the scan period.

[0033] In the above pixel circuit, the initial voltage is less than the difference between the first power supply voltage and a threshold voltage of the driving transistor.

[0034] In the above pixel circuit, the initial voltage is substantially equal to the second power supply voltage.

[0035] In the above pixel circuit, the compensation circuit includes a first transistor connected between the second node and an initial voltage node having the initial voltage, wherein the first transistor comprises a gate electrode configured to receive a first compensation control signal that is activated during the first compensation period. In the above pixel circuit, the compensation circuit further includes a second transistor connected between the second node and the third node and having a gate electrode configured to receive a second compensation control signal that is activated during the second compensation period.

[0036] In the above pixel circuit, the compensation circuit further includes a third transistor connected between the first node and a reference voltage node having a reference voltage, wherein the third transistor comprises a gate electrode configured to receive the first compensation control signal. In the above pixel circuit, the compensation circuit further includes a fourth transistor connected between the first node and the reference voltage node and having a gate electrode configured to receive the second compensation control signal.

[0037] In the above pixel circuit, the compensation circuit further includes a fifth transistor connected between the fourth node and the initial voltage node and having a gate electrode configured to receive the first compensation control signal or the second compensation control signal.

[0038] In the above pixel circuit, the driving transistor is configured to operate in a saturation region.

[0039] Another aspect is an electroluminescent display comprising a display unit including a plurality of pixel circuits arranged in rows and columns, wherein each pixel cir-

cuit includes a driving transistor including a gate electrode configured to be initialized to an initial voltage during a first compensation period and is configured to turn on the driving transistor during a second compensation period following the first compensation period. The electroluminescent display further comprises a data driver configured to provide data signals to the display unit, a scan driver configured to provide row control signals to the display unit, and a timing controller configured to control the display unit, the data driver and the scan driver.

[0040] In the above electroluminescent display, the scan driver is configured to generate and sequentially activate a plurality of compensation control signals. In the above electroluminescent display, the pixel circuits of a k-th row are configured to receive (k−1)-th and k-th compensation control signals. In the above electroluminescent display, each pixel circuit of the k-th row is configured to initialize the gate electrode to the initial voltage while the (k−1)-th compensation control signal is activated and turn on the driving transistor while the k-th compensation control signal is activated.

[0041] In the above electroluminescent display, the scan driver is configured to generate and sequentially activate first and second compensation control signals. In the above electroluminescent display, each of the pixel circuits is further configured to receive the first and second compensation control signals. In the above electroluminescent display, each pixel circuit is configured to initialize the gate electrode to the initial voltage while the first compensation control signal is activated and turn on the driving transistor while the second compensation control signal is activated.

[0042] In the above electroluminescent display, each pixel circuit includes a scan transistor connected between a data line and a first node and having a gate electrode configured to receive a scan signal, a first capacitor connected between a first power supply voltage and the first node, a second capacitor connected between the first node and a second node, an emission control transistor connected between a third node and a fourth node and having a gate electrode configured to receive an emission control signal, a light-emitting diode (LED) connected between the fourth node and a second power supply voltage less than the first power supply voltage, and a compensation circuit configured to initialize the second node to an initial voltage during the first compensation period and electrically connect the second node to the third node during the second compensation period, wherein the driving transistor is connected between the first power supply voltage and the third node, and wherein the gate electrode of the driving voltage is connected to the second node.

[0043] In the above electroluminescent display, the compensation circuit includes a first transistor having a gate electrode and connected between the second node and an initial voltage node having the initial voltage, wherein the gate electrode of the first transistor is configured to receive a first compensation control signal that is activated during the first compensation period. In the above electroluminescent display, the compensation circuit further includes a second transistor connected between the second node and the third node and having a gate electrode configured to receive a second compensation control signal that is activated during the second compensation period, a third transistor having a gate electrode and connected between the first node and a reference voltage node having a reference voltage, wherein the gate electrode of the third transistor is configured to receive the first compensation control signal. In the above electroluminescent display, the compensation circuit further includes a fourth transistor connected between the first node and the reference voltage node and having a gate electrode configured to receive the second compensation control signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0044] FIG. **1** is a circuit diagram illustrating a pixel circuit according to an example embodiment.

[0045] FIG. **2** is a timing diagram illustrating operations of the pixel circuit of FIG. **1**.

[0046] FIG. **3** is a block diagram illustrating an electroluminescent display according to an example embodiment.

[0047] FIG. **4** is a timing diagram illustrating operations of the electroluminescent display of FIG. **3**.

[0048] FIG. **5** is a diagram illustrating an example of driving the electroluminescent display of FIG. **3**.

[0049] FIG. **6** is a block diagram illustrating an electroluminescent display according to an example embodiment.

[0050] FIG. **7** is a timing diagram illustrating operations of the electroluminescent display of FIG. **6**.

[0051] FIG. **8** is a diagram illustrating an example of driving the electroluminescent display of FIG. **6**.

[0052] FIGS. **9** and **10** are diagrams for describing operational characteristics of a pixel circuit according to example embodiments.

[0053] FIGS. **11** and **12** are circuit diagrams illustrating a pixel circuit according to example embodiments.

[0054] FIG. **13** is a block diagram illustrating a mobile device according to example embodiments.

DETAILED DESCRIPTION

[0055] In a digital driving method for an electroluminescent display, a problem can occur where the quality of a displayed image degrades due to deviations of the threshold voltage of transistors included in pixels, a resistive drop (IR-drop) of power supply voltages, etc. Compensation circuits can correct this deficiency.

[0056] In this disclosure, the term "substantially" includes the meanings of completely, almost completely or to any significant degree under some applications and in accordance with those skilled in the art. Moreover, "formed on" can also mean "formed over." The term "connected" can include an electrical connection.

[0057] FIG. **1** is a circuit diagram illustrating a pixel circuit according to an example embodiment.

[0058] Referring to FIG. **1**, a pixel circuit **10** includes a scan transistor TS, a first capacitor C**1**, a second capacitor C**2**, a driving transistor TD, an emission control transistor TE, a light-emitting diode (LED) LD and a compensation circuit **20**.

[0059] The scan transistor TS is coupled between a data line DL and a first node N**1**, and a gate electrode of the scan transistor TS receives a scan signal SCN. The first capacitor C**1** is coupled between a first power supply voltage ELVDD and the first node N**1**. The second capacitor C**2** is coupled between the first node N**1** and a second node N**2**. The driving transistor TD is coupled between the first power supply voltage ELVDD and a third node N**3**. A gate electrode of the driving transistor TD is coupled to the second node N**2**. The emission control transistor TE is coupled between the third node N**3** and a fourth node N**4**. A gate electrode of the emission control transistor TE receives an emission control signal EM. The light-emitting diode LD is coupled between the

fourth node N4 and a second power supply voltage ELVSS that is less than the first power supply voltage ELVDD.

[0060] FIG. **1** illustrates an embodiment of using p-channel metal-oxide semiconductor (PMOS) transistors. For example, the signals applied to the gate electrodes of the PMOS transistors are activated with a logical low level. Some transistors can be replaced with n-channel metal-oxide semiconductor (NMOS) transistors and the signals applied to the gate electrodes of the NMOS transistors can be activated with a logical high level.

[0061] When the scan signal SCN is activated with a logical low level, the scan transistor TS is turned on and a data voltage DT on the data line DL is applied to the first node N**1**. The voltage on the second node N**2** depends on the data voltage DT when the driving transistor TD is turned on.

[0062] When the emission control signal EM is activated with the logical low level, the emission control transistor TE is turned on and a driving current is provided to the light-emitting diode LD depending on the data voltage DT. The on-off ratio of the light-emitting diode LD and brightness are determined by the driving current. The light-emitting diode LD can be any type, for example, an organic light-emitting diode (OLED).

[0063] The compensation circuit **20** initializes the second node N**2** to an initial voltage or initial voltage node VINT during a first compensation period PC**1** and electrically connects the second node N**2** to the third node N**3** during a second compensation period PC**2** after the first compensation period PC**1**.

[0064] As illustrated in FIG. **1**, the compensation circuit **20** includes a first transistor T**1**, a second transistor T**2**, a third transistor T**3** and a fourth transistor T**4**, but the compensation circuit **20** is not limited thereto.

[0065] The first transistor T**1** is coupled between the second node N**2** and the initial voltage VINT, and a gate electrode of the first transistor T**1** receives a first compensation control signal CMPa that is activated during the first compensation period PC**1**. The second transistor T**2** is coupled between the second node N**2** and the third node N**3**, and a gate electrode of the second transistor T**2** receives a second compensation control signal CMPb that is activated during the second compensation period PC**2**. Using the first and second transistors T**1** and T**2**, the second node N**2** can be initialized to an initial voltage VINT during the first compensation period PC**1**. Further, the second node N**2** and the third node N**3** can be electrically connected to each other during the second compensation period PC**2** after the first compensation period PC**1**.

[0066] The third transistor T**3** is coupled between the first node N**1** and a reference voltage or reference voltage node VREF, and a gate electrode of the third transistor T**3** receives the first compensation control signal CMPa. The fourth transistor T**4** is coupled between the first node N**1** and the reference voltage VREF, and a gate electrode of the fourth transistor T**4** receives the second compensation control signal CMPb. Using the third and fourth transistors T**3** and T**4**, the reference voltage VREF can be applied to the first node N**1** during the first compensation period PC**1** and the second compensation period PC**2**.

[0067] FIG. **2** is a timing diagram illustrating operations of the pixel circuit **10** of FIG. **1**.

[0068] Referring to FIG. **2**, each frame period PF can include the first compensation period PC**1**, the second compensation period PC**2** after the first compensation period PC**1**, and a scan-emission period PSE after the second compensation period PC**2**.

[0069] The first and second compensation control signals CMPa and CMPb are respectively activated with the logical low level during the first and second compensation periods PC**1** and PC**2**. The scan-emission period PSE can include a scan period and at least one emission period PE. During the scan period, the scan signal SCN is activated with the logical low level and the scan transistor TS is turned on. During the emission period PE, the emission control signal EM is activated at the logical low level and the emission control transistor TE is turned on.

[0070] The relative timings between the emission period and the scan period in each frame period PF can be determined according to different driving methods. For example, for a progressive emission scheme where the emission control transistors TE are turned on sequentially row by row, the scan period PS can be included in the emission period PE as illustrated in FIG. **2**. For example, the scan signal SCN can be activated to turn on the scan transistor TS while the emission control signal EM is activated to turn on the emission control transistor TE. The emission period PE can begin after the scan period PE in the progressive emission scheme. For a simultaneous emission scheme where the emission control transistors TE of all rows are turned on substantially simultaneously, the emission period PE has to begin after the scan period TS is finished with all of the rows.

[0071] Hereinafter, the operation of the pixel circuit **10** is further described with reference to FIGS. **1** and **2**. The operation of the pixel circuit **10** are divided into the first compensation period PC**1**, the second compensation period PC**2** and the scan-emission period PSE.

[0072] During the first compensation period PC**1**, the first compensation control signal CMPa is activated with the logical low level, and then the first and third transistors T**1** and T**3** are turned on. The second compensation control signal CMPb, the scan signal SCN and the emission control signal EM are deactivated with the logical high level, and then the scan transistor TS, the driving transistor TD, the emission control transistor TE, the second transistor T**2** and the fourth transistor T**4** are turned off. As a result, the reference voltage VREF is applied to the first node N**1** and the initial voltage VINT is applied to the second node N**2** during the first compensation period PC**1**. The initial voltage VINT can be set to be less than the first power supply voltage ELVDD subtracted by a threshold voltage VTH of the driving transistor TD, so that the driving transistor TD can be turned off. The initial voltage VINT can be set as a sufficiently low voltage, considering deviation of the threshold voltage of the driving transistor TD and boosting effect by the second capacitor C**2**. For example, the initial voltage VINT is set to the second power supply voltage ELVSS.

[0073] During the second compensation period PC**2**, the second compensation control signal CMPb is activated with the logical low level, and then the second and fourth transistors T**2** and T**4** are turned on. The first compensation control signal CMPa, the scan signal SCN and the emission control signal EM are deactivated with the logical high level, and then the scan transistor TS, the driving transistor TD, the emission control transistor TE, the first transistor T**1** and the third transistor T**3** are turned off. As a result, the reference voltage VREF is applied to the first node N**1**, and a diode-connection of the driving transistor TD is formed by electrically connect-

ing the second node N2 to the third node N3 during the second compensation period PC2. Through the diode-connection, the first power supply voltage ELVDD subtracted by the threshold voltage VTH of the driving transistor TD is applied to the second node N2.

[0074] During the scan-emission period PSE, the first and second compensation control signals CMPa and CMPb are deactivated with the logical high level, and then the first through fourth transistors T1 through T4 are turned off. The emission control signal EM is activated with the logical low level, and then the emission control transistor TE is turned on.

[0075] As will be described with reference to FIG. **5**, the frame period PF can include a plurality of scan-emission periods, for example, a plurality of sub-field driving periods. Each scan-emission period PSE can include a scan period PS for loading or programming a data bit to the first node N1. During the scan period PS, the scan signal SCN is activated with the logical low level to turn on the scan transistor TS and then the data voltage DT is applied to the first node N1. When the data voltage DT is applied to the first node N1, a voltage VB on the second node N2 is represented by Expression 1 by coupling of the second capacitor C2.

$$VB=(ELVDD-VTH+VDT-VREF) \quad \text{Expression 1}$$

[0076] In Expression 1, VB indicates the voltage at the second node N2, ELVDD indicates the first power supply voltage, VTH indicates the threshold voltage of the driving transistor TD, VDT indicates the data voltage programmed on the first node N1, and VREF indicates the reference voltage. The driving transistor TD operates in a saturation region as will be described with reference to FIG. **10**, and thus a current ITD through the driving transistor TD can be represented as Expression 2.

$$ITD = (1/2)*\mu*Cox*(W/L)*(ELVDD-VB-VTH)^2 \quad \text{Expression 2}$$
$$= (1/2)*\mu*Cox*(W/L)*(VREF-VDT)^2$$

[0077] In Expression 2, ITD indicates the current flowing through the driving transistor TD, μ indicates the mobility of charge carriers of the driving transistor TD, Cox indicates a gate capacitance of the driving transistor TD, and W/L indicates the width/length of the driving transistor TD.

[0078] The driving transistor TD is turned on when the data voltage VDT is less than the reference voltage VREF and the driving transistor TD is turned off when the data voltage VDT is greater than the reference voltage VREF. If the data voltage VDT is less than the reference voltage VREF, the current ITD through the driving transistor TD is represented as Expression 2 and thus the current ITD has a value independent of the threshold voltage VTH and the first power supply voltage ELVDD. If the data voltage VDT is greater than the reference voltage VREF, the current ITD has a value of substantially zero because the driving transistor TD is turned off.

[0079] The data voltage VDT can be set to the logical high level greater than the reference voltage VREF and the logical low level less than the reference voltage VREF to control the switching operation, that is, the on-off ratio of the driving transistor TD. When the driving transistor TD is turned on, the current ITD as Expresssion2 flows through the light-emitting diode LD. When the driving transistor TD is turned off, substantially no current flows through the light-emitting diode LD. Using such switching operation, the emission time of the light-emitting diode LD can be controlled through a pulse width modulation scheme to represent grayscales.

[0080] As such, the pixel circuit **10** can compensate for the gate voltage of the driving transistor TD by reflecting the operational characteristics of the pixel circuit **10**. The pixel circuit **10** can reduce variations of brightness of the displayed image due to deviations of the power supply voltage and the threshold voltage of the driving transistor TD. In addition, the pixel circuit **10** can reduce the variation of brightness due to temperature changes and degradation of the light-emitting diode LD since the driving transistor TD operates in the saturation region.

[0081] FIG. **3** is a block diagram illustrating an electroluminescent display according to an example embodiment.

[0082] Referring to FIG. **3**, an electroluminescent display **100** includes a display unit **110** and a driving unit. The driving unit includes a timing controller (TMC) **120**, a data driver (DDRV) **130** and a scan driver (SDRV) **140**. Even though not illustrated in FIG. **3**, the electroluminescent display **100** can further include a buffer for storing image data to be displayed, a voltage generator, etc.

[0083] The display unit **110** includes a plurality of pixel circuits PX that are arranged in rows and columns. For example, the pixel circuits PX are arranged in a matrix form of m rows and n columns. The display unit **110** is coupled to the data driver **130** through a plurality of data lines, and is coupled to the scan driver **140** through a plurality of row control lines.

[0084] As described with reference to FIGS. **1** and **2**, each pixel circuit PX can initialize the gate electrode of a driving transistor TD to the initial voltage VINT during the first compensation period PC1. Furthermore, each pixel circuit PX electrically connects the gate electrode to the drain electrode of the driving transistor TD during the second compensation period PC2 after the first compensation period PC1. Further, each pixel circuit PX can apply a reference voltage VREF to a first node N1 where the data bit is programmed during a scan period PS.

[0085] The data driver **130** provides data signals DT1~DTn to the display unit **110** through the data lines. The scan driver **140** provides row control signals to the display unit **110** through the row control lines. The row control signals include emission control signals EMP~EMm provided through emission control lines, scan signals SCN1~SCNm provided through scan lines, and compensation control signals CMP0~CMPm provided through compensation control lines. The pixel circuits PX can be located where the data lines and the scan lines cross.

[0086] The driving unit **120**, **130** and **140** can receive display data from an external device and drive the display unit **110** so as to display an image corresponding to the display data. For example, the driving unit **120**, **130** and **140** can drive the display unit **110** with a hybrid digital driving method. That is, the driving unit **120**, **130** and **140** can provide each pixel circuit PX in the display unit **110** with a data voltage (e.g., a voltage for turning on a driving transistor TD or a voltage for turning off the driving transistor TD) that allows the driving transistor TD to operate in a saturation region. The driving unit **120**, **130** and **140** can produce a grayscale by adjusting the time duration for which the pixel circuit PX emits light in each frame. Unlike a typical digital driving method in which a driving transistor of each pixel circuit operates in a linear region, in the hybrid digital driving method, the driving tran-

sistor TD of each pixel circuit PX operates in the saturation region, thereby increasing the lifespan of the pixel circuits PX.

[0087] The timing controller **120** can control overall operations of the electroluminescent display **100**. The timing controller **120** can provide control signals to control the display unit **110**, the data driver **130** and the scan driver **140**. In some embodiments, the timing controller **120**, the data driver **130** and the scan driver **140** can be implemented as a single integrated circuit (IC). In other embodiments, the timing controller **120**, the data driver **130** and the scan driver **140** can be implemented as two or more ICs.

[0088] As illustrated in FIG. **3**, the respective emission control signal EMk and the corresponding scan signal SCNk are provided to the pixel circuits PX of the corresponding k-th row. Among the plurality of compensation control signals CMP**0**~CPMm, the (k−1)-th compensation control signal CMPk−1 and the k-th compensation control signal CMPk are provided to the pixel circuits PX of the k-th row.

[0089] Hereinafter, the operation and the driving method of the electroluminescent display **100** are further described with reference to FIGS. **4** and **5**.

[0090] FIG. **4** is a timing diagram illustrating the operation of the electroluminescent display **100** of FIG. **3**. FIG. **5** is a diagram illustrating an example of driving the electroluminescent display **100** of FIG. **3**.

[0091] Referring to FIGS. **4** and **5**, the scan driver **130** generates a plurality of compensation control signals CMP**0**~CMPm that are activated sequentially during time intervals T**0**~Tm. Also, the scan driver **130** generates a plurality of scan signals SCN**1**~SCNm that are activated sequentially during time intervals T**2**~Tm+1.

[0092] A (k−1)-th compensation control signal CMPk−1 and a k-th compensation control signal CMPk among the plurality of compensation control signals CMP**0**~CMPm are provide to the pixel circuits PX of a k-th row. Referring to the pixel circuit **10** of FIG. **1**, the (k−1)-th compensation control signal CMPk−1 corresponds to the first compensation control signal CMPa and the k-th compensation control signal CMPk corresponds to the second compensation control signal CMPb. The k-th scan signal SCNk and the k-th emission control signal EMk correspond to the scan signal SCN and the emission control signal EM in FIG. **1**, respectively.

[0093] Each pixel circuit PX of the k-th row can initialize the gate electrode of the driving transistor TD to the initial voltage VREF while the (k−1)-th compensation control signal CMPk−1 is activated. for example, during the first compensation period PC**1**. In addition, each pixel circuit PX of the k-th row can electrically connect the gate electrode N**2** to the drain electrode N**3** of the driving transistor TD while the k-th compensation control signal CMPk is activated, for example, during the second compensation period PC**2**. Each pixel circuit PX of the k-th row can turn on the scan transistor TS to apply each data voltage to the first node N**1** while the k-th scan signal SCNk is activated, for example, during the scan period Ps that can be included in the scan-emission period PSE after the first and second compensation periods PC**1** and PC**2**.

[0094] For example, the pixel circuits of the first row can operate in response to the zero-th compensation control signal CMP**0**, the first compensation control signal CMP**1** and the first scan signal SCN**1**. For example, for the pixel circuits PX in the first row, the zero-th time interval T**0** corresponds to the first compensation period PC**1**, the first time interval T**1** corresponds to the second compensation period and the second time interval T**2** corresponds to the scan period PS. The pixel circuits of the second row can operate in response to the first compensation control signal CMP**1**, the second compensation control signal CMP**2** and the second scan signal SCN**2**. For example, for the pixel circuits PX in the second row, the first time interval T**1** corresponds to the first compensation period PC**1**, the second time interval T**2** corresponds to the second compensation period PC**2** and the third time interval T**3** corresponds to the scan period PS.

[0095] In this way, the voltage compensation operation can be performed sequentially row by row from the first row to the m-th row, and the scan operation can be performed sequentially row by row from the first row to the m-th row.

[0096] FIG. **5** illustrates the method of driving the electroluminescent display using the sequential voltage compensation operation and the sequential scan operation.

[0097] Referring to FIG. **5**, each frame period PF includes a compensation period PS and a plurality of scan-emission periods PSE**1**~PSE**3**. The compensation period PS can begin sequentially from the first row to the m-th row, and also the scan-emission periods PSE**1**~PSE**3** can begin sequentially from the first row to the m-th row after the compensation period PS. Each scan-emission period will be referred to as a sub-field driving period or a sub-frame driving period. The number of the scan-emission periods in each frame period PF can change variously.

[0098] FIG. **5** illustrates embodiments where the times of the emission periods PE**1**~PE**3** increase gradually. In other embodiments, the times of the emission periods PE**1**~PE**3** can decrease gradually. FIG. **5** illustrates embodiments of a progressive emission scheme where the emission period begins sequentially row by row. In other embodiments, the simultaneous emission scheme can be used such that the emission period begins at substantially the same time for all rows after the scan period is finished with respect to all rows.

[0099] Each of the scan-emission periods PSE**1**~PSE**3** can include each of the scan periods PS**1**~PS**3** and each of the emission periods PE**1**~PE**3**. As described above, each emission period PEi can begin after the corresponding scan period PSi is finished, or each scan period PSi can be included in the corresponding emission period PEi.

[0100] As described above, the compensation period PC includes the first compensation period PC**1** for initializing the gate voltage of the driving transistor TD and the second compensation period PC**2** for forming the diode-connection of the driving transistor TD.

[0101] As such, the method of driving the electroluminescent display including the pixel circuit according to example embodiments can compensate for the gate voltage of the driving transistor TD by reflecting the operational characteristics of the pixel circuit. This method reduces variations of brightness of the displayed image due to deviations of the power supply voltage and the threshold voltage of the driving transistor TD, temperature changes and degradation of the light-emitting diode LD, thereby enhancing quality of display image.

[0102] FIG. **6** is a block diagram illustrating an electroluminescent display according to an example embodiment.

[0103] Referring to FIG. **6**, an electroluminescent display **200** includes a display unit **210** and a driving unit. The driving unit includes a timing controller (TMC) **220**, a data driver (DDRV) **230** and a scan driver (SDRV) **240**. Even though not

illustrated in FIG. **6**, the electroluminescent display **200** can further include a buffer for storing image data to be displayed, a voltage generator, etc.

[0104] The display unit **210** includes a plurality of pixel circuits PX that are arranged in rows and columns. For example, the pixel circuits PX is arranged in a matrix form of m rows and n columns. The display unit **210** is coupled to the data driver **230** through a plurality of data lines, and is coupled to the scan driver **240** through a plurality of row control lines.

[0105] As described with reference to FIGS. **1** and **2**, each pixel circuit PX can initialize the gate electrode of the driving transistor TD to the initial voltage VINT during the first compensation period PC**1** and electrically connect the gate electrode to the drain electrode of the driving transistor TD during the second compensation period PC**2** after the first compensation period PC**1**. Further, each pixel circuit PX can apply the reference voltage VREF to the first node N**1** where the data bit is programmed during a scan period PS.

[0106] The data driver **230** provides data signals DT**1**~DTn to the display unit **210** through the data lines. The scan driver **240** provides row control signals to the display unit **110** through the row control lines. The row control signals include emission control signals EMP~EMm provided through emission control lines, scan signals SCN**1**~SCNm provided through scan lines, and first and second compensation control signals CMPa and CMPb provided through compensation control lines. The pixel circuits PX can be located where the data lines and the scan lines cross.

[0107] The driving unit **220**, **230** and **240** can receive display data from an external and drive the display unit **210** to display an image corresponding to the display data. For example, the driving unit **220**, **230** and **240** can drive the display unit **210** with a hybrid digital driving method in which the driving unit **220**, **230** and **240** provide each pixel circuit PX with a data voltage (e.g., a voltage for turning on a driving transistor TD or a voltage for turning off the driving transistor TD) that allows the driving transistor TD to operate in the saturation region. The driving unit **220**, **230** and **240** can produce a grayscale by adjusting the time duration for which the pixel circuit PX emits light in each frame. Unlike a typical digital driving method in which a driving transistor of each pixel circuit operates in the linear region, the display unit **210** can be driven with the hybrid digital driving method in which the driving transistor TD operates in the saturation region, thereby increasing the lifespan of the pixel circuits PX.

[0108] The timing controller **220** can control overall operations of the electroluminescent display **200**. The timing controller **220** can provide control signals to control the display unit **210**, the data driver **230** and the scan driver **240**. In some embodiments, the timing controller **220**, the data driver **230** and the scan driver **240** can be implemented as a single integrated circuit (IC). In other embodiments, the timing controller **220**, the data driver **230** and the scan driver **240** can be implemented as two or more ICs.

[0109] As illustrated in FIG. **6**, the emission control signal EMk and the corresponding scan signal SCNk are transmitted to the pixel circuits PX of the corresponding k-th row. The first and second compensation control signals CMPa and CMPb are provided commonly to the pixel circuits PX of all rows.

[0110] Hereinafter, the operation and the driving method of the electroluminescent display **200** are further described with reference to FIGS. **7** and **8**.

[0111] FIG. **7** is a timing diagram illustrating the operation of the electroluminescent display **200** of FIG. **6**. FIG. **8** is a diagram illustrating an example of driving the electroluminescent display **200** of FIG. **6**.

[0112] Referring to FIGS. **7** and **8**, the scan driver **230** generates the first and second compensation control signals CMPa and CMPb that are activated sequentially during time intervals T**0** and T**1**. Also the scan driver **230** generates a plurality of scan signals SCN**1**~SCNm that are activated sequentially during time intervals T**2**~Tm+1.

[0113] The first compensation control signal CMPa and the second compensation control signal CMPb are provided commonly to the pixel circuits PX of all rows. Referring again to the pixel circuit **10** of FIG. **1**, the first and second compensation signals CMPa and CMPb are common with respect to all rows. The k-th scan signal SCNk and the k-th emission control signal EMk correspond to the scan signal SCN and the emission control signal EM in FIG. **1**, respectively.

[0114] Each pixel circuit PX of all rows can initialize the gate electrode of the driving transistor TD to the initial voltage while the first compensation control signal CMPa is activated during the first compensation period PC**1**. In addition, each pixel circuit PX of all rows can electrically connect the gate electrode N**2** to the drain electrode N**3** of the driving transistor TD while the second compensation control signal CMPb is activated during the second compensation period PC**2**. Each pixel circuit PX of the k-th row can turn on the scan transistor TS so as to apply each data voltage to the first node N**1** while the k-th scan signal SCNk is activated during the scan period Ps that can be included in the scan-emission period PSE after the first and second compensation periods PC**1** and PC**2**.

[0115] For example, the pixel circuits of the first row can operate in response to the first compensation control signal CMPa, the second compensation control signal CMPb and the first scan signal SCN**1**. For example, when the pixel circuits PX of the first row, the zero-th time interval T**0** corresponds to the first compensation period PC**1**, the first and second time intervals T**1** and T**2** respectively corresponds to the second compensation period and the scan period PS. The pixel circuits of the second row can operate in response to the first compensation control signal CMPa, the second compensation control signal CMPb and the second scan signal SCN**2**. For example, for the pixel circuits PX of the second row, the zero-th time interval T**0** corresponds to the first compensation period PC**1**, the first time interval T**1** corresponds to the second compensation period PC**2**, and the third time interval T**3** corresponds to the scan period PS.

[0116] In this way, the voltage compensation operation can be performed substantially simultaneously with respect to all rows from the first row to the m-th row, and the scan operation can be performed sequentially row by row from the first row to the m-th row.

[0117] FIG. **8** illustrates the method of driving the electroluminescent display using the substantially simultaneous voltage compensation operation and the sequential scan operation.

[0118] Referring to FIG. **8**, each frame period PF includes a compensation period PS and a plurality of scan-emission periods PSE**1**~PSE**3**. The compensation period PS can begin substantially simultaneously with respect to all rows from the first row to the m-th row, and the scan-emission periods PSE**1**~PSE**3** can begin sequentially from the first row to the m-th row after the compensation period PS. Each scan-emis-

sion period will be referred to as a sub-field driving period or a sub-frame driving period. The number of the scan-emission periods in each frame period PF can be changed variously.

[0119] FIG. **8** illustrates embodiments where the times of the emission periods PE**1**~PE**3** increase gradually. In other embodiments, the times of the emission periods PE**1**~PE**3** decrease gradually. FIG. **8** illustrates embodiments of a progressive emission scheme where the emission period begins sequentially row by row, and the simultaneous emission scheme can be adopted in other embodiments such that the emission period begins at substantially the same time for all rows after the scan period is finished with all rows.

[0120] Each of the scan-emission periods PSE**1**~PSE**3** can include each of the scan periods PS**1**~PS**3** and each of the emission periods PE**1**~PE**3**. As described above, each emission period PEi can begin after the corresponding scan period PSi is finished, or each scan period PSi can be included in the corresponding emission period PEi.

[0121] As described above, the compensation period PC includes the first compensation period PC**1** for initializing the gate voltage of the driving transistor TD and the second compensation period PC**2** for forming the diode-connection of the driving transistor TD.

[0122] As such, the method of driving the electroluminescent display including the pixel circuit according to embodiments can compensate for the gate voltage of the driving transistor TD by reflecting the operational characteristics of the pixel circuit so as to reduce variations of brightness of the displayed image due to deviations of the power supply voltage and the threshold voltage of the driving transistor TD, temperature changes and degradation of the light-emitting diode LD, thereby enhancing quality of display image.

[0123] FIGS. **9** and **10** are diagrams for describing operational characteristics of a pixel circuit according to some embodiments.

[0124] FIG. **9** illustrates an example where the driving transistor TD operates in the linear region. FIG. **10** illustrates an example where the driving transistor TD operates in the saturation region. The curves C**11** and C**21** are current-voltage (I-V) curves representing the relationship between the current and the source-drain voltage of the driving transistor TD. The curves C**12** and C**22** are I-V curves of the normal light-emitting diode LD, and the curves C**13** and C**23** are I-V curves of the degenerated light-emitting diode LD.

[0125] Referring to FIG. **9**, the driving transistor TD operates in the linear region in the typical pixel circuit where the driving transistor is used as a switch. The current at the point P**11**, which is a crossing point of the curves C**11** and C**12**, flows through the light-emitting diode LD to emit light. The driving current changes very sensitively to change of the I-V characteristic of the light-emitting diode LD because the driving transistor TD operates in the linear region. When the light-emitting diode LD is degraded or the operation time is changed, the driving current is changed to the point P**12**. As illustrated in FIG. **9**, the amount d**1** of the driving current change is relatively large, and thus the brightness deviation of the light-emitting diode LD is increased.

[0126] Referring to FIG. **10**, the pixel circuit according to embodiments operates in the saturation region and thus the amount d**2** of the driving current change is relatively small. As such, the pixel circuit operating in the saturation region and the electroluminescent display including the pixel circuit can reduce the brightness deviation due to temperature changes and degradation of the light-emitting diode, thereby enhancing quality of display images.

[0127] FIGS. **11** and **12** are circuit diagrams illustrating a pixel circuit according to embodiments.

[0128] Referring to FIGS. **11** and **12**, each of pixel circuits **11** and **12** includes a scan transistor TS, a first capacitor C**1**, a second capacitor C**2**, a driving transistor TD, an emission control transistor TE, a light-emitting diode LD and each of compensation circuits **21** and **22**.

[0129] The scan transistor TS is coupled between a data line DL and a first node N**1**. A gate electrode of the scan transistor TS receives a scan signal SCN. The first capacitor C**1** is coupled between a first power supply voltage ELVDD and the first node N**1**. The second capacitor C**2** is coupled between the first node N**1** and a second node N**2**. The driving transistor TD is coupled between the first power supply voltage ELVDD and a third node N**3**. A gate electrode of the driving transistor TD is coupled to the second node N**2**. The emission control transistor TE is coupled between the third node N**3** and a fourth node N**4**, and a gate electrode of the emission control transistor TE receives an emission control signal EM. The light-emitting diode LD is coupled between the fourth node N**4** and a second power supply voltage ELVSS that is less than the first power supply voltage ELVDD.

[0130] As described with reference to FIG. **1**, each of the compensation circuits **21** and **22** includes a first transistor T**1**, a second transistor T**2**, a third transistor T**3** and a fourth transistor T**4**, bus the compensation circuits **21** and **22** are not limited thereto.

[0131] The first transistor T**1** is coupled between the second node N**2** and the initial voltage VINT. A gate electrode of the first transistor T**1** receives a first compensation control signal CMPa that is activated during the first compensation period PC**1**. The second transistor T**2** is coupled between the second node N**2** and the third node N**3**, and a gate electrode of the second transistor T**2** receives a second compensation control signal CMPb that is activated during the second compensation period PC**2**. Using the first and second transistors T**1** and T**2**, the second node N**2** can be initialized to an initial voltage VINT during the first compensation period PC**1**. Also, using the first and second transistors T**1** and T**2**, the second node N**2** and the third node N**3** can be electrically connected to each other during the second compensation period PC**2** after the first compensation period PC**1**.

[0132] The third transistor T**3** is coupled between the first node N**1** and a reference voltage VREF. A gate electrode of the third transistor T**3** receives the first compensation control signal CMPa. The fourth transistor T**4** is coupled between the first node N**1** and the reference voltage VREF. A gate electrode of the fourth transistor T**4** receives the second compensation control signal CMPb. Using the third and fourth transistors T**3** and T**4**, the reference voltage VREF can be applied to the first node N**1** during the first compensation period PC**1** and the second compensation period PC**2**.

[0133] As illustrated in FIGS. **11** and **12**, the compensation circuit **21** further includes a fifth transistor T**5** coupled between the fourth node N**4** and the initial voltage VINT. In the embodiment of FIG. **11**, a gate electrode of the fifth transistor T**5** receives the first compensation control signal CMPa. In the embodiment of FIG. **12**, a gate electrode of the fifth transistor T**5** receives the second compensation control signal CMPb. Using the transistor T**5**, the initial voltage VINT can be applied to the fourth node N**4** during the first

compensation period PC1 or during the second compensation period PC2. When the driving voltage TD is turned off, such initialization of the fourth node N4 to the relatively low initial voltage VINT can reduce noises due to remaining charges at the third node N3.

[0134] FIG. **13** is a block diagram illustrating a mobile device according to example embodiments.

[0135] Referring to FIG. **13**, a mobile device **700** includes a processor **710**, a memory device **720**, a storage device **730**, an input/output (I/O) device **740**, a power supply **750**, and an electroluminescent display **760**. The mobile device **700** can further include a plurality of ports for communicating a video card, a sound card, a memory card, a universal serial bus (USB) device, or other electronic systems.

[0136] The processor **710** can perform various computing functions or tasks. The processor **710** can be for example, a microprocessor, a central processing unit (CPU), etc. The processor **710** can be connected to other components via an address bus, a control bus, a data bus, etc. Further, the processor **710** can be coupled to an extended bus such as a peripheral component interconnection (PCI) bus.

[0137] The memory device **720** can store data for operations of the mobile device **700**. For example, the memory device **720** can include at least one non-volatile memory device such as an erasable programmable read-only memory (EPROM) device, an electrically erasable programmable read-only memory (EEPROM) device, a flash memory device, a phase change random access memory (PRAM) device, a resistance random access memory (RRAM) device, a nano-floating gate memory (NFGM) device, a polymer random access memory (PoRAM) device, a magnetic random access memory (MRAM) device, a ferroelectric random access memory (FRAM) device, and/or at least one volatile memory device such as a dynamic random access memory (DRAM) device, a static random access memory (SRAM) device, a mobile dynamic random access memory (mobile DRAM) device, etc.

[0138] The storage device **730** can be, for example, a solid state drive (SSD) device, a hard disk drive (HDD) device, a CD-ROM device, etc. The I/O device **740** can be, for example, an input device such as a keyboard, a keypad, a mouse, a touch screen, and/or an output device such as a printer, a speaker, etc. The power supply **750** can supply power for operating the mobile device **700**. The electroluminescent display **760** can communicate with other components via the buses or other communication links.

[0139] As described above with reference to FIGS. **1** through **12**, the electroluminescent display **760** includes a plurality of pixel circuits such that each pixel circuit is configured to initialize a gate electrode of a driving transistor to an initial voltage during a first compensation period and electrically connect the gate electrode to a drain electrode of the driving transistor during a second compensation period after the first compensation period.

[0140] The present embodiments can be applied to any mobile device or any computing device. For example, the present embodiments can be applied to a cellular phone, a smart phone, a tablet computer, a personal digital assistant (PDA), a portable multimedia player (PMP), a digital camera, a music player, a portable game console, a navigation system, a video phone, a personal computer (PC), a server computer, a workstation, a tablet computer, a laptop computer, etc.

[0141] The foregoing is illustrative of example embodiments and is not to be construed as limiting thereof. Although a few example embodiments have been described, those skilled in the art will readily appreciate that many modifications are possible in the example embodiments without materially departing from the novel teachings and advantages of the inventive technology. Accordingly, all such modifications are intended to be included within the scope of the present inventive concept as defined in the claims. Therefore, it is to be understood that the foregoing is illustrative of various example embodiments and is not to be construed as limited to the specific example embodiments disclosed, and that modifications to the disclosed example embodiments, as well as other example embodiments, are intended to be included within the scope of the appended claims.

What is claimed is:

1. A pixel circuit for an electroluminescent display, comprising:

a scan transistor connected between a data line and a first node and having a gate electrode configured to receive a scan signal;

a first capacitor connected between a first power supply voltage and the first node;

a second capacitor connected between the first node and a second node;

a driving transistor connected between the first power supply voltage and a third node and having a gate electrode connected to the second node;

an emission control transistor connected between the third node and a fourth node and having a gate electrode configured to receive an emission control signal;

a light-emitting diode (LED) connected between the fourth node and a second power supply voltage less than the first power supply voltage; and

a compensation circuit configured to i) initialize the second node to an initial voltage during a first compensation period and ii) electrically connect the second node to the third node during a second compensation period following the first compensation period.

2. The pixel circuit of claim **1**, wherein the compensation circuit is further configured to apply a reference voltage to the first node during the first and second compensation periods.

3. The pixel circuit of claim **2**, wherein the driving transistor is configured to be turned on when a data voltage on the data line is less than the reference voltage, and wherein the driving transistor is configured to be turned off when the data voltage is greater than the reference voltage.

4. The pixel circuit of claim **1**, wherein the compensation circuit is further configured to apply the initial voltage to the fourth node during the first or second compensation period.

5. The pixel circuit of claim **1**, wherein the first and second compensation periods and a scan period after the second compensation period are defined as a frame period of the electroluminescent display, and wherein the scan transistor is configured to be turned on during the scan period.

6. The pixel circuit of claim **1**, wherein the initial voltage is less than the difference between the first power supply voltage and a threshold voltage of the driving transistor.

7. The pixel circuit of claim **1**, wherein the initial voltage is substantially equal to the second power supply voltage.

8. The pixel circuit of claim **1**, wherein the compensation circuit includes:

a first transistor connected between the second node and an initial voltage node having the initial voltage, wherein the first transistor comprises a gate electrode configured

to receive a first compensation control signal that is activated during the first compensation period; and

a second transistor connected between the second node and the third node and having a gate electrode configured to receive a second compensation control signal that is activated during the second compensation period.

9. The pixel circuit of claim **8**, wherein the compensation circuit further includes:

a third transistor connected between the first node and a reference voltage node having a reference voltage, wherein the third transistor comprises a gate electrode configured to receive the first compensation control signal; and

a fourth transistor connected between the first node and the reference voltage node and having a gate electrode configured to receive the second compensation control signal.

10. The pixel circuit of claim **9**, wherein the compensation circuit further includes:

a fifth transistor connected between the fourth node and the initial voltage node and having a gate electrode configured to receive the first compensation control signal or the second compensation control signal.

11. The pixel circuit of claim **1**, wherein the driving transistor is configured to operate in a saturation region.

12. An electroluminescent display comprising:

a display unit including a plurality of pixel circuits arranged in rows and columns, wherein each pixel circuit i) includes a driving transistor including a gate electrode configured to be initialized to an initial voltage during a first compensation period and ii) configured to turn on the driving transistor during a second compensation period following the first compensation period;

a data driver configured to provide data signals to the display unit;

a scan driver configured to provide row control signals to the display unit; and

a timing controller configured to control the display unit, the data driver and the scan driver.

13. The electroluminescent display of claim **12**, wherein the scan driver is configured to generate and sequentially activate a plurality of compensation control signals.

14. The electroluminescent display of claim **13**, wherein the pixel circuits of a k-th row are configured to receive (k−1)-th and k-th compensation control signals.

15. The electroluminescent display of claim **14**, wherein each pixel circuit of the k-th row is configured to i) initialize the gate electrode to the initial voltage while the (k−1)-th compensation control signal is activated and ii) turn on the driving transistor while the k-th compensation control signal is activated.

16. The electroluminescent display of claim **12**, wherein the scan driver is configured to generate and sequentially activate first and second compensation control signals.

17. The electroluminescent display of claim **16**, wherein each of the pixel circuits is further configured to receive the first and second compensation control signals.

18. The electroluminescent display of claim **17**, wherein each pixel circuit is configured to i) initialize the gate electrode to the initial voltage while the first compensation control signal is activated and ii) turn on the driving transistor while the second compensation control signal is activated.

19. The electroluminescent display of claim **12**, wherein each pixel circuit includes:

a scan transistor connected between a data line and a first node and having a gate electrode configured to receive a scan signal;

a first capacitor connected between a first power supply voltage and the first node;

a second capacitor connected between the first node and a second node;

an emission control transistor connected between a third node and a fourth node and having a gate electrode configured to receive an emission control signal;

a light-emitting diode (LED) connected between the fourth node and a second power supply voltage less than the first power supply voltage; and

a compensation circuit configured to i) initialize the second node to an initial voltage during the first compensation period and ii) electrically connect the second node to the third node during the second compensation period,

wherein the driving transistor is connected between the first power supply voltage and the third node, and wherein the gate electrode of the driving voltage is connected to the second node.

20. The electroluminescent display of claim **19**, wherein the compensation circuit includes:

a first transistor having a gate electrode and connected between the second node and an initial voltage node having the initial voltage, wherein the gate electrode of the first transistor is configured to receive a first compensation control signal that is activated during the first compensation period;

a second transistor connected between the second node and the third node and having a gate electrode configured to receive a second compensation control signal that is activated during the second compensation period;

a third transistor having a gate electrode and connected between the first node and a reference voltage node having a reference voltage, wherein the gate electrode of the third transistor is configured to receive the first compensation control signal; and

a fourth transistor connected between the first node and the reference voltage node and having a gate electrode configured to receive the second compensation control signal.

* * * * *

专利名称(译)	像素电路和包括其的电致发光显示器		
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摘要(译)

公开了一种像素电路和包括该像素电路的电致发光显示器。在一个方面，像素电路包括连接在数据线和第一节点之间并且具有被配置为接收扫描信号的栅电极的扫描晶体管，连接在第一电源电压和第三节点之间并具有栅极的驱动晶体管电极连接到第二节点，发射控制晶体管连接在第三节点和第四节点之间，并且具有配置为接收发射控制信号的栅电极，连接在第四节点和第二电源电压之间的发光二极管在第一补偿周期期间，补偿电路在第一补偿周期期间将第二节点初始化为初始电压，并且在第一补偿周期之后的第二补偿周期期间将第二节点电连接到第三节点。